

charge or discharge storage capacitor 132-11 of memory cell 112-11 to represent binary data. For a read operation, bit line BL-1 of array 110 is equilibrated with bit line BL-1*. Data stored in memory cell 112-11, as represented by the charge on its storage capacitor 132-11, is coupled to bit line BL-1 of array 110. The difference in charge in bit line BL-1 and bit line BL-1* is amplified, and a corresponding voltage level is provided to the input/output circuits.

Figures 2 through 4 illustrate an embodiment of a memory cell with a vertical transistor and trench capacitor for use, for example, in memory device 100 of Figure 1. Specifically, Figure 2 is a plan view of a layout of a number of memory cells indicated generally at 202A through 202D in array 200. Figure 2 depicts only four memory cells. It is understood, however, that array 200 may include a larger number of memory cells even though only four are depicted here.

Each memory cell is constructed in a similar manner. Thus, only memory cell 202C is described herein in detail. Memory cell 202C includes pillar 204 of single crystal semiconductor material, e.g., silicon, that is divided into [first] second source/drain region 206, body region 208, and [second] first source/drain region 210 to form access transistor 211.

On page 10, please make the following changes.

Pillar 204 extends vertically outward from substrate 212 of, for example, p- silicon.

[First] Second source/drain region 206 and [second] first source/drain region 210 each comprise, for example, n + silicon and body region 208 comprises p- silicon.

Word line 212 passes body region 208 of access transistor 211 in isolation trench 214. Word line 212 is separated from body region 208 of access transistor 211 by gate oxide 216 such that the portion of word line 212 adjacent to body region 208 operates as a gate for access transistor 211. Word line 212 may comprise, for example, n+ poly-silicon material that is deposited in isolation trench 214 using an edge-defined technique such that word line 212 is less than a minimum feature size, F, for the lithographic technique used to fabricate array 200. Passing word line 213 is also formed in trench 214. Cell 202C is coupled with cell 202B by bit line 218.

Memory cell 202C also includes storage capacitor 219 for storing data in the cell. A first plate of capacitor 219 for memory cell 202C is integral with [second] first source/drain region 210 of access transistor 211. Thus, memory cell 202C may be more easily realizable when compared to conventional vertical transistors since there is no need for a contact between [second] first source/drain region 210 and capacitor 219. Second plate 220 of capacitor 219 is common to all of the capacitors of array 200. Second plate 220 comprises a mesh or grid of n+ poly-silicon formed in deep trenches that surrounds at least a portion of [second] first source/drain region 210 of each pillar 204A through 204D. Second plate 220 is grounded by contact with substrate 212 underneath the trenches. Second plate 220 is separated [from] first source/drain region 210 by gate oxide 222.

With this construction for memory cell 202C, access transistor 211 is like a silicon on insulator device. Three sides of the transistor are insulated by thick oxide in the shallow trench. If the doping in pillar 204 is low and the width of the post is sub-micron, then body region 208 can act as a “fully-depleted” silicon on insulator transistor with no body or substrate to contact. This is desirable to avoid floating body effects in silicon on insulated transistors and is achievable due to the use of sub-micron dimensions in access transistor 211.

On page 11, please make the following changes.

Figure 4 is a schematic diagram that illustrates an effective circuit diagram for the embodiment of Figures 2 and 3. It is noted that storage capacitor 219 formed by [second] first source/drain region 210 and second plate 220 is depicted as four separate capacitors. This represents that the [second] first plate 220 surrounds second source/drain region 210 which increases the charge storage capacitance and stored charge for the memory cell. It is also noted that second plate 220 is maintained at a constant potential, e.g., ground potential.

As shown in Figure 2, the memory cells of array 200 are four-square feature ($4F^2$) memory cells. Using cell 202D as an example, the surface area of cell 202D is calculated based on linear dimensions in the bit line and word line directions. In the bit line direction, the distance from one edge of cell 202D to a common edge of adjacent cell 202A is approximately 2 minimum feature sizes ($2F$). In the word line direction, the dimension is taken from the midpoint

of isolation trenches on either side of memory cell 202D. Again, this is approximately two minimum feature sizes (2F). Thus, the size of the cell is $4F^2$. This size is much smaller than the current cells with stacked capacitors or trenched capacitors.

Figures 5A through 5M illustrate one embodiment of a process for fabricating an array of memory cells, indicated generally at 299, according to the teachings of the present invention. In this example, dimensions are given that are appropriate to a 0.2 micrometer lithographic image size. For other image sizes, the vertical dimensions can be scaled accordingly.

As shown in Figure 5A, the method begins with substrate 300. Substrate 300 comprises, for example, a P-type silicon wafer, layer of P- silicon material, or other appropriate substrate material. Layer 302 is formed, for example, by epitaxial growth outwardly from layer 300. Layer 302 comprises single crystalline N+ silicon that is approximately 3.5 micrometers thick. Layer 304 is formed outwardly from layer 302 by epitaxial growth of single crystalline P- silicon of approximately 0.5 microns. Layer 306 is formed by ion implantation of donor dopant into layer 304 such that layer 306 comprises single crystalline N+ silicon with a depth of approximately 0.1 microns.

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. Specific amendments to individual claims are detailed in the following marked up set of claims.

Please amend the claims as follows:

20. (Once Amended) A method of fabricating a memory array, the method comprising the steps of:

forming a number of access transistors, each access transistor formed in a pillar of semiconductor material that extends outwardly from a substrate wherein [the] each access transistor includes, in order, a first source/drain region, a unitary body region and a second source/drain region formed vertically thereupon;

forming a trench capacitor, wherein a first plate of the trench capacitor is integral with the